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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BONZO, BRYCE P	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,266	OKBAY ET AL.	
	Examiner	Art Unit	
	Bryce P. Bonzo	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-17,19-21,23-27 and 29-32* is/are rejected.

7)☒ Claim(s) *5,18,22 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non-Final Official Action

Status of the Claims

Claims 1, 2, 4, 6, 15-17, 20, 21, 23-25, 27 and 29-32 are rejected under 35 USC §102.

Claims 3, 7-17, 19 and 26 are rejected under 35 USC §103.

Claims 5, 18, 22 and 28 are objected to while containing allowable subject matter.

Petitions

In view of the papers filed 4/19/04, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by adding the named inventor.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of Office records to reflect the inventorship as corrected.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 6, 15-17, 20, 21, 23-25, 27 and 29-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohashi (United States Patent Application Publication No. US 2004/0078690 A1).

As per claim 1, Kohashi discloses:

An apparatus for logging diagnostic information, the apparatus comprising:

at least one software module configured to provide diagnostic information to a bus (¶1);

a plurality of buffers configured to store data (¶23-25);

a buffer management module configured to transfer diagnostic information from the bus to a selected buffer of the plurality of buffers (¶24) and

the buffer management module further configured to transfer the diagnostic information from the selected buffer to a diagnostic log corresponding to the selected buffer (¶73).

2. The apparatus of claim 1, wherein the plurality of buffers are configured as a plurality of First In First Out (FIFO) memory devices (¶23).

4. The apparatus of claim 1, wherein the buffer management module is further configured to transfer variable-length diagnostic information from the bus to the selected buffer (Figure 10, shows zero padding for variable length data).

6. The apparatus of claim 1, wherein the buffer management module is further configured to transfer the diagnostic information from a selected buffer to the diagnostic log without consuming processor cycles (this is inherent as the processor is not responsible for the transfer),

Claims 15, 16, 17 and 20 are the computer readable storage medium embodiments of claims 1, 2, 4 and 6 respectively and are rejected accordingly.

Claims 21 and 23 are the means plus function embodiments of claims 1 and 6 respectively and are rejected accordingly.

Claims 24, 25, 27 and 29 are the system embodiment of claims 1, 2, 4 and 6 respectively and are rejected accordingly.

Claim 30 is the method embodiment of claim 1 and is rejected accordingly.

Claims 31 and 32 are the FIFO management module of claims 1 and 6 respectively and are rejected accordingly.

Rejections under 35 USC §03

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7-14, 19, 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohashi (United States Patent Application Publication No. US 2004/0078690 A1).

As per claim 3, Kohashi does not explicitly disclose:

The apparatus of claim 1, wherein the plurality of buffers are configured as a plurality of circulating buffer memory devices.

Official Notice is taken that is it notoriously well known to use circular buffers, a class of FIFO buffers, in high speed logging. Circular buffers offer the benefit of in the event of a filling of the buffer continuing to record the most recent data at the expense of order data. These types of buffers are generally used in high speed systems so that as much data as possible can be saved, and generally have high input and output speeds. Thus it would have been obvious to one of ordinary skill in the art of debugging to circular buffers as the FIFOs of Kohashi and thus allowed the high speed logging of the bus.

As per claim 7, Kohashi does not explicitly disclose:

The apparatus of claim 1, wherein the diagnostic log resides within a processor-accessible memory.

Official Notice is given that it is notoriously well known to store logs in memory spaces accessible by processors. This is often done to allow the processor to aid in analysis or transport. Additionally, logs are often stored in processor memory simply because it is unused memory near the processor which is not currently used thus reducing the amount of additionally dedicated debugging hardware designed into the chip. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the storing of logs in processor accessible memory to save space on the chip and potentially allow for the processor in Kohashi to aid in it the log analysis.

As per claim 8, Kohashi does not explicitly disclose:

The apparatus of claim 1, wherein the diagnostic log resides within a multiple-use memory.

Official Notice is given that it is notoriously well known by those skilled in the art to allow diagnostic logs to be reside multiple-use memory. Often this memory is what is referred to system memory. System memory is generally very large regions of intermediate speed RAM. This memory is designed to be used for many operations, temporarily buffering data awaiting transit elsewhere, being one of its functions. Thus it would have

been obvious to one of ordinary skill in the art at the time of invention to store diagnostic logs in multiple use memory thereby avoiding the designing and integration of additional diagnostic only memory into a system, thus saving space and cost while designing a chip.

As per claim 9, Kohashi does not explicitly disclose:

The apparatus of claim 1, further comprising a decoder module configured to match a bus state with at least one tracing pattern register.;

Official Notice is given that it is notoriously well known to store a bus state pattern in memory. This is most often done in to trigger the beginning or ending of a trace. Traces can be very large data sets and as such triggering the start and stop of trace provides the benefit or reducing the size of the data set prior to and after the period of interest. Thus it would have been obvious to one of ordinary skill in the art at the tome of invention to incorporate the well known practice of triggering into the system of Kohashi thus allowing the data generated by Kohashi to be smaller, and thus easier to manage.

As per claim 10, Kohashi does not explicitly disclose:

The apparatus of claim 1, wherein the bus is a processor data bus.

Official notice is given that it is notoriously well known to place data of interest on a processor bus. The processor is the workhorse of a computer, and as such the data which directly enters the processor is of key interest. Numerous system have been designed to monitor both the instruction and data buses of processors in order to determine why processors act in aberrant fashion. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the well know practice of monitoring a process bus into the diagnostic system of Kohashi thus providing additional process detail for use in debugging.

As per claim 11, Kohashi does not disclose:

The apparatus of claim 1, further comprising a control register configured to store a starting address of a selected buffer.

Official Notice is given that is it notoriously well known to provide and store the starting address of memory regions. Many memory spaces require allocation, as opposed to hardwire connections, to apportion and partition large blocks of unassigned memory. Without these starting addresses it would be impossible to ever locate the data stored to memory after it was stored. Thus it would have been obvious to one of ordinary skill in the art at the time of invention store the starting addresses in Kohashi thus allowing the user to recover the data and allow for analysis.

As per claim 12, Kohashi not explicitly disclose:

The apparatus of claim 1, further comprising a control register configured to store an extent of a selected buffer.

Official Notice is given that it is notoriously well known to store the extend of a memory region. This is done so that the memory management system can prevent overflows, provide garbage collection, use a variety of indexed based pointer addressing schemes, and determine how full the memory is. Without the information for the extent, most modern memory system will fail. System memory in modern computers in particular operates using this information. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the well known practice of storing the extent of a memory region into the system of Kohashi in order to prevent the implicit problems with using a memory region with no known bounds.

As per claim 13, Kohashi does not explicitly disclose:
The apparatus of claim 1, further comprising a control register configured to store a starting address of a diagnostic log associated with a selected buffer

Official Notice is given that is it notoriously well known to provide and store the starting address of memory regions. Many memory spaces require allocation, as opposed to hardwire connections, to apportion and partition large blocks of unassigned memory. Without these starting addresses it would be impossible to ever locate the data stored to memory after it was stored. Thus it would have been obvious to one of ordinary skill in

the art at the time of invention store the starting addresses in Kohashi thus allowing the user to recover the data and allow for analysis.

As per claim 14, Kohashi does not explicitly disclose:
The apparatus of claim 1, further comprising a control register configured to store an extent of a diagnostic log associated with a selected buffer.

Official Notice is given that it is notoriously well known to store the extend of a memory region. This is done so that the memory management system can prevent overflows, provide garbage collection, use a variety of indexed based pointer addressing schemes, and determine how full the memory is. Without the information for the extent, most modern memory system will fail. System memory in modern computers in particular operates using this information. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the well known practice of storing the extent of a memory region into the system of Kohashi in order to prevent the implicit problems with using a memory region with no known bounds.

Claim 19 is the computer readable storage medium embodiment of claim 3 and is rejected accordingly.

Claim 26 is system embodiment of claim 3 and is rejected accordingly.

Allowable Matter

Claims 5, 18, 22 and 28 are indicated as containing allowable subject matter. These claims describe the process of moving data from the bus to buffers in response to a cache line flush. It is the use of this particular trigger in this very specific logging system that has over come the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bryce P. Bonzo

Bryce P Bonzo
Primary Examiner
Art Unit 2113